ESSDERC Tutorial

Silicon-on-Insulator: From materials to Circuit Design

Content: This tutorial will cover different aspects of SOI technology, ranging form substrate preparation to circuit design. The Smart-Cut technique has enabled the mass production of SOI wafers, but is also a powerful technique for the formation of hybrid substrates and for More the Moore applications. The particular properties of SOI MOSFETs can be used to improve circuit speed or electrical performance. These properties will be reviewed and compact models for SOI MOSFETs will be presented. Design techniques and tools for analogue, digital and RF applications will be described.

Organiser: J.P. Colinge, Tyndall National Institute, Ireland

Topic	Lecturer	Time
Smart-cut enabled materials	C Colinge (Tyndall)	9:30 - 10:30
BREAK		10:30 – 11:00
Physics of SOI devices	JP Colinge (Tyndall)	11:00 - 12:00
SOI MOSFET compact models	B Iniguez (URV)	12:00 - 13:00
LUNCH		13:00 - 14:30
SOI Design: RF	JP Raskin (UCL)	14:30 - 15:30
BREAK		15:30 - 15:45
SOI design: analog	D Flandre (UCL)	15:45 - 16:45
SOI design: logic circuits	Ph Flatresse (STM)	16:45 - 17:45

Lecture 1: Smart-cut® enabled materials

The simplicity and success of direct wafer bonding coupled with ex-foliation (Smart Cut®) has made it possible to transfer thin, single crystal materials to any substrate. An example of Smart Cut® is silicon on insulator (SOI) which is used for a variety of microelectronic applications. Furthermore, Smart Cut® enables the integration of exotic materials such as III-V semiconductors or Ge with any substrate. In this talk I will discuss the basic Smart Cut® technique used for SOI and then describe other variations of Smart Cut® and their applications.

Instructor: Professor **Cindy Colinge** received her Bachelor of Science in Chemical Engineering 1983 from University of California, Davis, the Master of Science in Electrical and Electronic Engineering 1989 from California State University, Sacramento, and the Doctor of Philosophy in Electrical Engineering 1993 University of California, Davis working on bond and etch-back silicon on insulator. From August 1993 to 2009 she has held the position of Professor in the department of Electrical Engineering at California State University, Sacramento. She is currently at Tyndall National Institute in Cork, Ireland where she is studying interfacial properties of bonded heterostructures. Professor Colinge has written and presented over 50 articles on wafer bonding and has co-authored a textbook on "Physics of Semiconductor Devices. She is a Senior Member of IEEE since 2003 and a Member Electrochemical Society 1990. She has been and continues to be a member of the organizing committee for the Electrochemical Society's International Symposium on Semiconductor Wafer Bonding Science, Technology, and Application.

Lecture 2: Physics of the SOI transistor

This lecture will compare the physics of bulk MOSFETs, partially depleted SOI MOSFETs and fully depleted SOI MOSFETs. Emphasis is placed on the properties that make these devices interesting for particular applications. For instance, one can take advantage of PDSOI's floating-body effects to increase the speed of digital circuits. The superior linearity of FDSOI is excellent for analog applications, high-resistivity SOI wafers are well adapted to the fabrication of RF devices.

Instructor: Prof. **Jean-Pierre Colinge** received a BS degree in Philosophy, the Electrical Engineer degree, and the Ph.D. degree in Applied Sciences from the Université catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980, and 1984, respectively. He worked at the Centre National d'Etudes des Télécommunications (CNET), Meylan, France, at the Hewlett-Packard Laboratories, Palo Alto, USA, at IMEC, Leuven, Belgium, where he was involved in SOI technology for VLSI and special device applications. From 1991 to 1997, Dr. Colinge was professor at the Université catholique de Louvain, leading a research team in the field of SOI technology for low-power, radiation-hard, high-temperature and RF applications as well as reduced dimension devices (thin double-gate and quantum-wire MOSFETs). He has published over 340 scientific papers and four books on the field of SOI as well as two books on semiconductor device physics. Prof. Colinge is currently Professor at the Tyndall National Institute, University College Cork, Ireland, where he is head of the Micro-Nano Electronics Centre and is conducting research on modelling, fabrication and characterization of advanced SOI MOS devices.

Lecture 3: Compact Modeling of the SOI MOSFET

The goal of this lecture is to present compact modeling techniques which have been applied for different types of thin film SOI and multiple-gate MOSFETs: Ultra-Thin Body SOI MOSFETs, Double-Gate MOSFETs, Gate AllAround MOSFETs, Tri-Gate MOSFETs, and FinFETs. Long channel models areobtained by deriving a unified charge control model from the solution the 1-D Poisson's equation (considering volume inversion), and using an appropriate and self-consistent transport model. The final channel current, charge and capacitance models are written in terms of the charge sheet densities at the source and drain ends of the channel. The short-channel effects have to be incorporated to the compact models. Analytical and scalable models for the subthreshold swing, threshold voltage roll-off and DIBL have been developed by solving the 2-D or 3-D Poisson equation using a number of appropriate techniques. Quasi-static small-signal models, with analytical expressions for transconductances, conductances and capacitances, can be developed from the derived charge control model. Finally, using the active transmission line approach, the quasi-static compact models can be extended to the high frequency operation, in order to study the RF performance, including noise. Explicit expressions for the noise parameters can be developed.

Instructor: **Benjamin Iñíguez** received the B. S., the M. S. and the Ph. D. Degrees in physics fromthe University of the Balearic Islands (UIB), Spain, in1989, 1992 and 1996, respectively. His doctoral research focused on thedevelopment of CAD models for short-channel bulk-Si and SOI MOSFETs. FromFebruary 1997 to September 1998 he was working as a Postdoctoral ResearchScientist at the ECSE Department, Rensselaer Polytechnic Institute (RPI), Troy, NY, in 1997-98, wherehe studied advanced devices, such as short-channel a-Si and poly-Si TFTs, GaNHFETs and heterodimensional MESFETs. From September 1998 to February 2001 hewas a Research Scientist (Postdoctoral Marie-Curie Grant Holder) in theMicroelectronics Laboratory, Université catholique de Louvain (UCL),Louvain-la-Neuve, Belgium, working on the characterization and modeling ofthin-film and ultrathin-film SOI MOSFETs from DC to RF conditions. In February2001 he joined the Department of Electronic Engineering (DEEEA), UniversitatRovira i Virgili (URV), Tarragona, Spain, as Titular Professor. In 2004 he was awarded the Distinction of theCatalan Government for the Promotion of University Research. In 2007 heobtained the IET Premium Award for a paper about charge transport in organicTFTs. His current research interests are characterization and modeling ofadvanced electron devices, in particular nanoscale SOI and multiple-gate MOSFETs andorganic and polymer TFTs. He is IEEE Senior Member from 2003, and IEEE EDSDistinguished Lecturer since 2004. In 2009 he obtained the ICREA Academia Prize. In 2010 he became Full Professor at the UniversitatRovirai Virgili (URV). HE has authored or co-authored more than 80 papers ininternational journals and a similar number in internationalconferences. He has participated in several European projects, and heis the leader of the "COMON" (Compact Modelling Network), an IndustryAcademia Pertnership and Pathway funded by the 7th Framework Programmeof the European Commission.

Lecture 4: Analog SOI CMOS : devices figures of merit, design techniques and applications

Substrate insulation is responsible for SOI-specific MOS behaviour, whether advantageous (such as reduced body effect or capacitances) or detrimental such as static, dynamic and frequency-dependent floating-body effects or self heating. Their significant impacts on analog device properties and performance will be reviewed. The design and experimental results of low-power thin-film SOI CMOS analog blocks will be comprehensively presented and compared to bulk Si, targeting applications from micropower to very high-frequency, high-precision or high-temperature specifications and emphasizing SOI design tips and optimization opportunities. An Ultra-Low-Power (ULP) design technique will also be presented.

Instructor: **Denis Flandre** is Professor at Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium. Since 1986, he has been working on the modelling and characterization of SOI MOS devices and automated synthesis methodology for MOS analog circuits. He is now involved in R&D of SOI MOS devices, digital and analog circuits, as well as sensors and MEMS, for special applications (high-speed, low-voltage low-power, microwave, biomedical, rad-hard and high-temperature electronics and microsystems). He has co-authored more than 500 technical papers. He is co-inventor of 10 patents. He has organized or lectured many short courses on SOI technology, devices and circuits in universities, industries and conferences. He is director of the UCL Micro/nano-technology facility (Winfab.be), an executive of EU Networks of excellence (EUROSOI, HITEN (for High-Temperature Electronics), NANOSIL) and virtual institute (SINANO (on Silicon Nano-devices)), an IEEE Senior member, a member of the SOI Industry Consortium and a co-founder of CISSOID S.A., a spin-off company of UCL founded in 2000, focusing on SOI high-temperature IC solutions.

Lecture 5: SOI technology: an opportunity for RF designers?

Modern communication systems are very demanding; high frequency, high degree of integration, low power consumption, and they have to present good performance even under harsh environment. The integrability and power consumption reduction of the digital part will further improve with the continued downscaling of technologies. The bottleneck for further advancement is the analog front-end.
This last decade Silicon-on-Insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency reaching cut-off frequencies close to 500 GHz for nMOSFETs and for harsh environments (high temperature, radiations) commercial applications. Partially Depleted SOI is now massively serving the 45-nm digital market where it is seen as a low cost - low power alternative to bulk silicon. Fully depleted devices are also widely spread as they outperform existing semiconductor technologies for extremely low power analog applications.
For RF and systems-on-chip applications, SOI also presents the major advantage of providing high resistivity substrate capabilities, leading to substantially reduced substrate losses. Substrate resistivity values higher than 1 kΩ.cm can easily be achieved and High Resistivity Silicon is commonly foreseen as a promising substrate for radio frequency integrated circuits (RFIC) and mixed signal applications. Based on several experimental and simulation results the interest, limitations but also possible future improvements of the SOI MOS technology for RF applications are presented.

Instructor: **Jean-Pierre Raskin** received the Industrial Engineer degree from the Institut Supérieur Industriel d'Arlon, Belgium, in 1993, and the M.S. and Ph.D. degrees in Applied Sciences from the Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1994 and 1997, respectively. In 1998, he joined the EECS Department of The University of Michigan, Ann Arbor, USA. In 2000, he joined the Microwave Laboratory of UCL, Louvain-la-Neuve, Belgium, as Associate Professor. Since 2007, he has been a Full Professor and Head of the Microwave Laboratory of UCL. He was visiting professor at The University of Newcastle, Newcastle Upon Tyne, UK, for one year from September 2009. His research interests are the modeling, wideband characterization and fabrication of advanced SOI MOSFETs, micro and nanofabrication of MEMS/NEMS sensors and actuators as well as the characterization of intrinsic properties of materials at nanoscale. He is an IEEE Senior Member, EuMA Associate Member and Member of the Research Center in Micro and Nanoscopic Materials and Electronic Devices of the Université catholique de Louvain. He has published more than 150 articles in international journals and over 300 articles in conference proceedings.

Lecture 6: SOI design for low-power applications

The trade-off between performance and power consumption is the major challenge on the horizon for scaling of CMOS ICs. SOI technology offers solutions to this challenge and is receiving today strong interest from the semiconductor industry. However, the lack of design knowledge and IP libraries lead the list of missing pieces for a wide SOI adoption.
The lecture intends to show that a SOI digital design platform dedicated to low power applications can be derived from its bulk counterpart at a low cost design effort. The efficiency of such approach will be demonstrated on standard cells, SRAM, IO libraries and low power solutions ... Comparisons between SOI and BULK based on silicon measurements and circuit simulations will be presented, showing the advantages of SOI in the low power arena.

Instructor: **Philippe Flatresse** received the PhD degree in Microlectronics from the Institut National Polytechnique de Grenoble in 1999. During his thesis, he developed LETISOI spice model dedicated to partially depleted SOI circuits at CEA-LETI, the R&D laboratory from French Atomic Energy Commission, located in Grenoble. In year 2000, he joined STMicroelectronics Central R&D, Crolles, where is currently in charge of CMOS Design Platforms qualification and digital SOI design in Central CAD and Design Solutions department. Dr. Flatresse has coauthored more than 40 papers and filed 10 patents in advanced CMOS technologies.